WE CLAIM

1. A circuit for monitoring information put onto an interconnect by one or more modules, said circuit comprising:
circuitry for determining if the information on the interconnect matches one or more conditions; and
circuitry for preventing a module from putting further information onto said interconnect if it is determined that information on the interconnect matches said one or more conditions.

2. A circuit as claimed in claim 1, wherein said information comprises packets of information.

3. A circuit as claimed in claim 1, wherein said information comprises requests and responses.

4. A circuit as claimed in claim 1, wherein said circuitry for preventing a module from putting further information onto the interconnect comprises a register.

5. A circuit as claimed in claim 4, wherein the register comprises one bit for each module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect.

6. A circuit as claimed in claim 4, wherein a location is defined in said register for each module, the location being independent of the address of the module used by the interconnect.

7. A circuit as claimed in claim 1, wherein the module which puts the information onto the interconnect which matches the one or more conditions is prevented by the preventing

circuitry from being granted access to the interconnect.

8. A circuit as claimed in claim 1, wherein the determining circuitry comprises comparator circuitry which compares the information on the interconnect with one or more match conditions.

9. A circuit as claimed in claim 1, wherein said conditions comprise one or more preconditions and one or more match conditions, said circuitry for preventing a module from putting information onto said interconnect being arranged to preventing said module from putting information onto said interconnect when said one or more preconditions and said one more match conditions occur.

10. A circuit as claimed in claim 9, wherein one precondition is that the one or more match conditions have occurred a predetermined number of times.

11. A circuit as claimed in claim 9, wherein one precondition is that the circuit is enabled.

12. A circuit as claimed in claim 9, wherein one precondition is that circuitry external to said circuit has been enabled.

13. A circuit as claimed in claim 12, wherein said external circuitry is a latch.

14. A circuit as claimed in claim 9, wherein said match conditions comprise one or more of the following:
an address or address range of the information;
the module or modules which put the information onto the interconnect;
the module or modules which are intended to receive the information on the interconnect; and

the type of transaction to which the information relates.

15. A circuit as claimed in any preceding claim, wherein storing circuitry is provided to store the information which satisfies the at least one condition.

16. A circuit comprising:
an interconnect;
one or more modules connected to the interconnect; and
a circuit for monitoring information put onto the interconnect by one or more modules, said circuit comprising:
circuitry for determining if the information on the interconnect matches one or more conditions; and
circuitry for preventing a module from putting further information onto said interconnect if it is determined that information on the interconnect matches said one or more conditions.

17. A circuit as claimed in claim 16, wherein the circuit is an integrated circuit.

18. A circuit as claimed in claim 16, wherein an arbiter is provided for arbitrating between the modules to determine which module is granted access to the interconnect at a given time, said arbiter being connected to the preventing circuitry, the arbiter and the preventing circuitry being arranged so that a module which is prevented from putting further information onto the interconnect is prevented from winning an arbitration.

19. A circuit as claimed in claim 18, wherein said determining circuitry is at least partially in the arbiter.

20. A circuit as claimed in claim 16, wherein said interconnect is a bus.

21. A circuit as claimed in claim 16, wherein one of said modules comprises a debug module.

22. A circuit as claimed in claim 16, wherein said preventing circuit is in said debug module.

23. A circuit as claimed in claim 22, wherein at least part of the determining circuitry is in the debug module.

24. A circuit comprising:
an interconnect;
one or more modules connected to the interconnect to put information onto the interconnect;
an arbiter for determining which module is permitted to put information onto the interconnect; and
circuitry for preventing a module from putting further information onto said interconnect, said preventing circuitry preventing a module from winning an arbitration carried out by said arbiter.

25. A method comprising the steps of:
monitoring information on an interconnect, the information being put onto the interconnect by one or modules;
determining if the information on an interconnect satisfies one or more conditions; and
preventing a module from putting information onto an interconnect if it is determined that the information satisfies one or more conditions.